Seda Ogrenci Memik

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University of California – Los Angeles
Ph.D., Computer Science Department *August 2003*

Northwestern University
M.S., Electrical and Computer Engineering Department *May 2000*

Bogazici University, Istanbul, Turkey
B.S., Department of Electrical and Electronic Engineering *July 1998*

Director, Computer Engineering Division
Professor, Department of Electrical and Computer Engineering
Professor, Department of Computer Science

Associate Professor, Dept. of Electrical Engineering and Computer Science, September 2009 – August 2016
Assistant Professor, Dept. of Electrical Engineering and Computer Science, September2003-September2009

AWARDS AND HONORS

1. Best Teacher in EECS Academic Year 2012-2013.
2. Distinguished Visitor, School of Computer Science, Complutense Universidad de Madrid, March-May 2010.
3. Best Paper Award Finalist, IEEE/ACM International Conference on Computer Aided Design (ICCAD) 2007
4. National Science Foundation CAREER Award (2006)
5. Searle Center for Teaching Excellence Junior Fellow (2006-2007)
6. International VLSID Design Conference, Pune, India, January 2018, **Best PhD Student Forum Presentation Award**
7. Best Paper Award Nomination, IEEE/ACM Design Automation Conference (DAC) 2005
8. Best Paper Award Nomination, IEEE/ACM Design Automation Conference (DAC) 2001

RECENT PUBLICATIONS

Book

Heat Management in Integrated Circuits: On-Chip and System-Level Monitoring and Cooling, S. Ogrenci-Memik, The Institution of Engineering and Technology, *2016*

Refereed Journal Publications

1. A.M.C. Deiana, N. Tran, J. Agar, M. Blott, G. Di Guglielmo, J. Duarte, P. Harris, S. Hauck, M. Liu, M. S. Neubauer, J. Ngadiuba, S. Ogrenci-Memik, M. Pierini, et al., **Applications and techniques for fast machine learning in science**, Frontiers in Big Data, Volume 5, 2022.
2. G. Di Guglielmo, F. Fahim, C. Herwig, M.B. Valentin, J. Duarte, C. Gingu, P. Harris, J. Hirschauer, M. Kwok, V. Loncar, Y. Luo, L. Miranda, J. Ngadiuba, D. Noonan, S. Ogrenci-Memik, M. Pierini, S. Summers, N. Tran, **A reconfigurable neural network ASIC for detector front-end data compression at the HL-LHC**, IEEE Transactions on Nuclear Science 68 (8), 2179-2186, 2021.
3. Y. Luo, J. C. Zhao, A. Aggarwal, S. Ogrenci-Memik, and K. Yoshii, **Thermal Management for FPGA Nodes in HPC Systems**, ACM Transactions on Design Automation of Electronic Systems 26, 2, Article 14, December 2020
4. G. Deptuch, J. Hoff, S. Jindariani, S. Joshi, D. Li, T. Liu, S. Ogrenci-Memik, J. Olsen, N. Tran, **Performance Study of the First 2D Prototype of Vertically Integrated Pattern Recognition Associative Memory (VIPRAM)**, IEEE Transactions on Nuclear Science, 67(9), pp. 2111-2118, September 2020
5. X. Yang, M. Grayson, S. Ogrenci-Memik, **Micro-scale 2D Thermal Gradiometer**, IEEE Electron Device Letters, 41(5), pp. 761-764, March 2020

6. F. Fahim, S. Joshi, S. Ogrenci-Memik, H. Mohseni, **A Low Power, High Speed Readout for Pixel Detectors based on an Arbitration Tree**, IEEE Transactions on VLSI, 28(2), pp. 576-584, February 2020
7. AA Del Barrio, R Hermida, S Ogrenci-Memik, **A Combined Arithmetic-High-Level Synthesis Solution to Deploy Partial Carry-Save Radix-8 Booth Multipliers in Datapaths**, IEEE Transactions on Circuits and Systems I: Regular Papers, Vol. 66(2), pp. 742-755, 2018
8. S. Joshi, D. Li, S. Ogrenci-Memik, G. Deptuch, J. Hoff, S. Jindariani, T. Liu, J. Olsen, N. Tran, **Multi-Vdd Design for Content Addressable Memories (CAM): A Power-Delay Optimization Analysis**, Journal of Low Power Electronics and Applications, 8(3), 25, 2018
9. A. Guliani, K. Zhang, S. Ogrenci-Memik, G. Memik, K. Kazutomo, R. Sankaran, P. Beckman, **Machine Learning-Based Temperature Prediction for Runtime Thermal Management across System Components**, IEEE Transactions on Parallel and Distributed Systems, 29(2), pp. 405—419, 2018
10. D. Li, S. Joshi, J. Kim, S. Ogrenci-Memik, **End-to-end Analysis of Integration for Thermocouple-based Sensors into 3D ICs**, IEEE Transactions on VLSI, Volume 25, Issue: 9, pp. 2498-2511, Sept. 2017.

Refereed Conference/Workshop Publications

1. A Narayanan, J Arnold, M Austin, JR Berlioz, P Hanlet, KJ Hazelwood, MA Ibrahim, VP Nagaslaev, DJ Nicklaus, G Pradhan, PS Prieto, BA Schupbach, K Seiya, A Saewert, RM Thurman-Keup, NV Tran, D Ulusel, J Jiang, H Liu, S Memik, R Shi, M Thieme, **Machine learning for slow spill regulation in the fermilab delivery ring for mu2e,** 5th North American Particle Acceleration Conference, 2022.
2. M. Thieme, J. Arnold, M. Austin, P. Hanlet, K. Hazelwood, M. Ibrahim, H. Liu, S. Memik, V. Nagaslaev, A. Narayanan, D. Nicklaus, G. Pradhan, A. Saewert, B. Schupbach, K. Seiya, R. Shi, R. Thurman-Keup, N. Tran, **Semantic Regression for Disentangling Beam Losses in the Fermilab Main Injector and Recycler,** North American Particle Acceleration Conference, 2022.
3. F. Fahim, L. Carloni, G. Di Guglielmo, C. Herwig, J. F. Hirschauer, Y. Luo, S. Ogrenci-Memik, N. Tran, **High-Level Synthesis to On-chip Implementation of a Reconfigurable AI Accelerator for Front- end Data Analysis at the HL-LHC**, IEEE Nuclear Science Symposium & Medical Imaging Conference (NSS-MIC), 2020
4. C. Herwig, L. Carloni, G. Di Guglielmo, F. Fahim, B. Hawks, J. F. Hirschauer, M. Kwok, Y. Luo, D. Noonan, S. Ogrenci-Memik, N. Tran, **Design of a reconfigurable autoencoder algorithm for detector front-end ASICs**, IEEE Nuclear Science Symposium & Medical Imaging Conference (NSS-MIC), 2020
5. S. Joshi, S. Ogrenci-Memik, J. Hoff, T. Liu, Workload Dependent Power Estimation of Associative Memory based Tracking Triggers, Nuclear Science Symposium, Sidney, Australia, November 2018
6. Y. Luo, X. Wang, S. Ogrenci-Memik, G. Memik, K. Yoshii, P. Beckman, "Minimizing Thermal Variation in Heterogeneous HPC Systems with FPGA Nodes", IEEE International Conference on Computer Design (ICCD), Orlando, FL, October 2018
7. S. Joshi, S. Ogrenci-Memik, J. Hoff, T. Liu, "Power Characterization and Optimization of 3D Content Addressable Memories for Tracking Triggers", IEEE International VLSID Design Conference, PhD Forum, Pune, India, January 2018, **Best PhD Student Presentation Award**
8. Y. Luo, X. Wen, K. Yoshii, S. Ogrenci-Memik, G. Memik, H. Finkel, F. Capello, "Evaluating HPC Workloads with Irregular Memory Access Patterns", International Conference on Field Programmable Logic (FPL), September 2017.
9. D. Li, K. Zhang, A. Guliani, S. Ogrenci-Memik, "Adaptive Thermal Management for 3D ICs with Stacked DRAM Caches", Design Automation Conference (DAC), June 2017.
10. Y. Luo, S. Ogrenci-Memik, J. Gu, "Cell-to-Array Thermal-Aware Analysis of Stacked RRAM", International Symposium on Circuits and Systems (ISCAS) Baltimore, MD, May 2017.
11. S Joshi, D. Li, S Ogrenci-Memik, J Hoff, S Jindariani, T Liu, J Olsen, G. Deptuch, N Tran, "A Content Addressable Memory with Multi-Vdd Scheme for Low Power Tunable Operation", 60th International IEEE MWSCAS, 2017.

Patents

1. System and Method for Tracking Content in a Medicine Container, *Provisional Application Submitted, January 21, 2015*, Serial No. 62/105,966, Sanjay Mehrotra, Seda Ogrenci-Memik, Ilya Mikhelson
2. Bimetallic Integrated On-Chip Thermocouple Array, U.S. Patent Number: 8,517,605, August 27, 2013, NU Reference Number: NU2009-146-02 (29146), Inventors: Matthew A. Grayson, Seda Memik, Jieyi Long, Chuanle Zhou, Andrea Grace Klock

PROFESSIONAL ACTIVITIES

- Editorial Boards
  - Associate Editor, ACM Transactions on Reconfigurable Technology and Systems (TRETS), December 2022-present
  - Associate Co-Editor, IET Journal on Cyber-Physical Systems: Theory & Applications, Special Issue Title: Cyber-physical systems for medical and life sciences applications, Q4 2017
  - IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Associate Editor, Jan. 2007-2013
  - International Journal on Reconfigurable Computing, April 2011-present
- Co-Organizer, FastML For Science Workshop at IEEE/ACM International Conference on CAD, Nov 1, 2023
- Co-Organizer, Cross-Layer Architectures to Circuits Summer School, August 9-12, 2022, Evanston, IL
- Co-Organizer, Workshop on Enabling Transformative Advances in Energy and Quantum Materials through Development of Novel Approaches to Electron Microscopy, funded by NSF, September 2020
- Co-Organizer, CRA-W Cross-Layer Computing Summer School, August 15-17, 2018, Evanston, IL
- Co-Organizer, Workshop on FPGAs for Scientific Simulation and Data Analytics, (co-organized with Argonne Labs and National Center for Supercomputing Applications), October 12-14, 2016, Urbana, IL
- Program Co-Chair, International Conference on Embedded and Ubiquitous Computing (EUC)- 2015
- Visiting Scholar, Argonne National Labs, Spring Quarter 2014 (Northwestern Argonne Institute of Science and Engineering, Mini-Sabbatical Program)
- Conference Organizing Committee

  - Publication Chair, International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2015

  - Poster Chair, 21st Reconfigurable Architectures Workshop (RAW) 2013

  - Publicity Co-Chair, International Symposium on Field Programmable Logic and Its Applications (FPL) 2010

  - Local Arrangements Co-Chair for the Great Lakes Symposium on VLSI (GLSVLSI) 2005
- Leadership in Technical Program Committees (TPCs)

  - *Design Automation Track Chair*, Embedded and Ubiquitous Computing Conference (EUC), 2013, 2014

  - *Design Automation Track Chair*, Asia South Pacific Quality Electronic Design (ASQED) 2010, 2011, 2012

  - *VLSI-CAD Track Co-Chair*, International Symposium on VLSI (ISVLSI) 2009

  - *System Design Track Chair*; IEEE/ACM International Conference on Computer Aided Design (ICCAD) (2007)

  - *High-Level Synthesis Track Chair*; IEEE/ACM International Conference on Computer Aided Design (ICCAD) (2006)
- TPC Membership

  - Ninth International Workshop on Heterogeneous High-performance Reconfigurable Computing at the Supercomputing Conference, 2023

  - The International Symposium on Computer Architecture (ISCA) 2022

  - IEEE/ACM Design Automation Conference (DAC) 2013, 2014, 2015, 2018, 2019, 2020 (Track Co-chair), 2021(Track Co-chair)

  - Extended Review Committee, International Symposium on Computer Architecture (ISCA) 2019

  - International Conference on Microelectronic Devices and Technologies, 2018

  -IEEE/ACM International Conference on Computer Aided Design (ICCAD) 2004-2007, 2011-2013, 2023

  -Design, Automation and Test in Europe (DATE) 2006, 2015, 2016

  -International Conference on High Performance and Embedded Architectures and Compilers (HiPEAC) 2011

  -International Symposium on Field Programmable Logic and Its Applications (FPL) 2005-2017

  -Reconfigurable Architectures Workshop (RAW) 2008-2017

  -Great Lakes Symposium on VLSI (GLSVLSI) 2004-2009

  -Applied Reconfigurable Computing (ARC) Workshop (ARC) 2007-2017

  -Southern Conference on Programmable Logic (SPL) 2008-2012